

Features

- Low Power Consumption: 60uA (Typ)
- Maximum Output Current: 500mA
- Small Dropout Voltage
100mV@100mA (Vout=3.3V)
- PSRR=75dB@1KHz
- Input Voltage Range: 2.0V~8.0V
- Output Voltage Range: 1.2V~3.6V
(customized on command in 0.1V steps)
- Standby Current : less than 1μA
- High Accurate: ±2%
- Good Transient Response
- Over-Temperature Protection
- Support Fixed Output Voltage
- Output Current Limit
- Stable with Ceramic Capacitor
- Available Package
SOT23-5 \ DFN1x1-4
- RoHS Compliant and Lead (Pb) Free

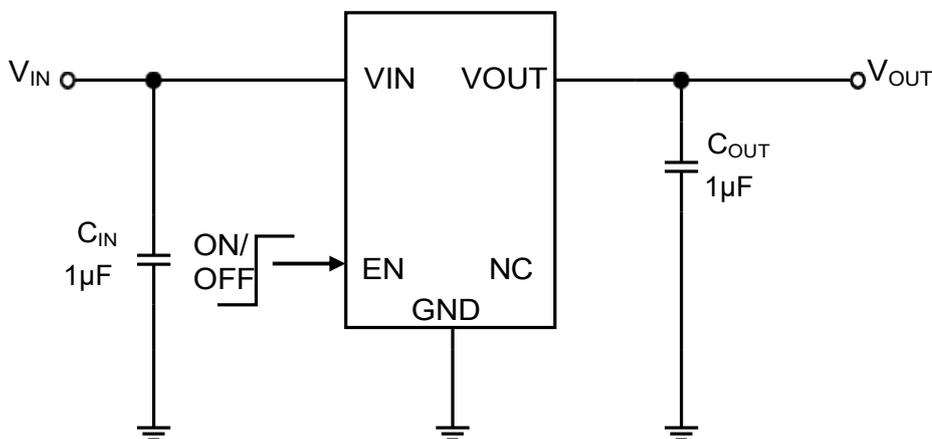
Application

- Portable, Battery Powered Equipment
- Audio/Video Equipment
- Power Management of MP3. PDA.....
- Weighting Scales. Home Automation

Description

The HE2211 series are highly precise, low noise, positive voltage LDO regulators manufactured using CMOS processes. The series achieves high ripple rejection and low dropout and consists of a standard voltage source, an error correction, current limiter and a phase compensation circuit plus a driver transistor. Output voltage is selectable in 0.1V increments within a range of 1.2V ~ 3.6V. The series is also compatible with low ESR ceramic capacitors which give added output stability. This stability can be maintained even during load fluctuations due to the excellent transient response of the series. The limiter's feedback circuit also operates as a protect for the output current limiter The EN function enables the output to be turned off, resulting in greatly reduced power consumption. The HE2211 consumes less than 1μA in shutdown mode and has fast turn-on time less than 50s. The other features include ultra low dropout voltage, high output accuracy, current limiting protection, and high ripple rejection ratio.

Application Circuits



Selection Table

Part No.	Output Voltage	Package	Marking
HE2211A12M5R	1.2V	SOT23-5	Refer to Marking rule
HE2211A15M5R	1.5V		
HE2211A18M5R	1.8V		
HE2211A25M5R	2.5V		
HE2211A28M5R	2.8V		
HE2211A30M5R	3.0V		
HE2211A33M5R	3.3V		
HE2211A36M5R	3.6V		
HE2211A12D4R	1.2V	DFN1x1-4	
HE2211A15D4R	1.5V		
HE2211A18D4R	1.8V		
HE2211A25D4R	2.5V		
HE2211A28D4R	2.8V		
HE2211A30D4R	3.0V		
HE2211A33D4R	3.3V		
HE2211A36D4R	3.6V		

Package and Pin assignment

SOT23-5 (Top View)

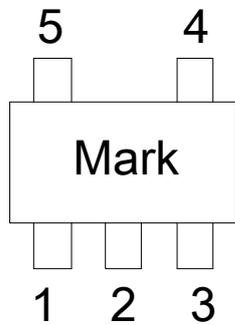


Table1: HE2211AXXM5R series (SOT23-5 PKG)

PIN NUMBER	SYMBOL	FUNCTION
1	V_{IN}	Power Input Pin
2	GND	Ground
3	CE	Chip Enable Pin
4	NC	No Connection
5	V_{OUT}	Output Pin

DFN1x1-4L (Top View)

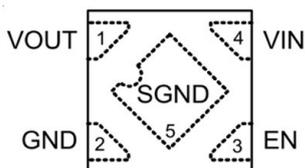


Table2: HE2211AXXD4R series (DFN1*1-4LPKG)

PIN NUMBER	SYMBOL	FUNCTION
1	V_{OUT}	Output Pin
2	GND	Ground
3	CE	Chip Enable Pin
4	V_{IN}	Power Input Pin
5	SGND	Substrate of Chip. Leave floating or tie to GND

Absolute Maximum Ratings ^{(1) (2)}

Parameter		Symbol	Maximum Rating	Unit
Input Voltage		V_{IN}	$V_{SS} - 0.3 \sim V_{SS} + 8.0$	V
		$V_{ON/OFF}$	$V_{SS} - 0.3 \sim V_{IN} + 0.3$	V
Output Current		I_{OUT}	600	mA
Output Voltage		V_{OUT}	$V_{SS} - 0.3 \sim V_{IN} + 0.3$	V
Power Dissipation	SOT23-5	P_d	250	mW
	DFN1x1-4		400	
Thermal Resistance	SOT23-5	$R_{\theta JA}^{(3)}$ (Junction-to-ambient thermal resistance)	400	$^{\circ}C/W$
	DFN1x1-4		250	$^{\circ}C/W$
Operating Temperature		T_{opr}	-40~85	$^{\circ}C$
Storage Temperature		T_{stg}	-40~125	$^{\circ}C$
Soldering Temperature & Time		T_{solder}	260 $^{\circ}C$, 10s	

Note (1): Exceeding these ratings may damage the device.

Note (2): The device is not guaranteed to function outside of its operating conditions

Note (3): The package thermal impedance is calculated in accordance to JESD 51-7.

ESD Ratings

Item	Description	Value	Unit
$V_{(ESD-HBM)}$	Human Body Model (HBM) ANSI/ESDA/JEDEC JS-001-2014 Classification, Class: 2	± 4000	V
$V_{(ESD-CDM)}$	Charged Device Mode (CDM) ANSI/ESDA/JEDEC JS-002-2014 Classification, Class: C0b	± 400	V
$I_{LATCH-UP}$	JEDEC STANDARD NO.78E APRIL 2016 Temperature Classification, Class: I	± 200	mA

ESD testing is performed according to the respective JESD22 JEDEC standard. The human body model is a 100 pF capacitor discharged through a 1.5k Ω resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin.

Recommended Operating Conditions

Parameter	MIN.	MAX.	Units
Supply voltage at V_{IN}	2.0	8.0	V
Operating junction temperature range, T_j	-40	125	$^{\circ}C$
Operating free air temperature range, T_A	-40	85	$^{\circ}C$

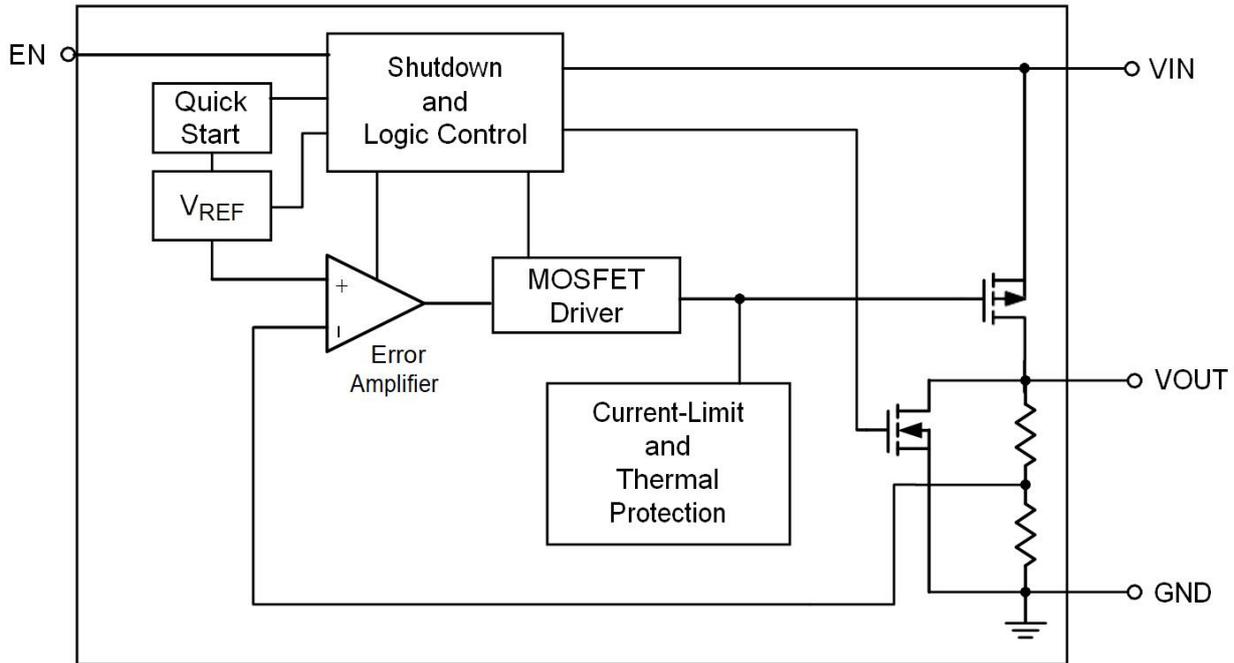
Note : All limits specified at room temperature ($T_A = 25^{\circ}C$) unless otherwise specified. All room temperature limits are 100% production tested. All limits at temperature extremes are ensured through correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

Electrical Characteristics

(Test Conditions: $V_{IN}=4.3V$, $V_{OUT}=3.3V$, $C_{IN}=1\mu F$, $C_{OUT}=1\mu F$, $T_A=25^\circ C$, unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Voltage	V_{IN}		-0.3		8.0	V
Supply Current	I_Q	$V_{IN} > V_{OUT}$, $EN = V_{IN}$ $I_{LOAD} = 0mA$	—	60	—	μA
Standby Current	I_{STBY}	$V_{EN} = GND$, Shutdown	—	1	—	μA
Output Voltage	V_{OUT}	$V_{IN} = V_{set} + 1.0V$ $I_{OUT} = 40mA$	$V_{set} * 0.98$	V_{set}	$V_{set} * 1.02$	V
Maximum Output Current	$I_{OUT(Max)}$	$V_{IN} = V_{OUT} + 1.0V$	—	500	—	mA
Dropout Voltage	V_{DROP}	$I_{OUT} = 100mA$	—	100	—	mV
		$I_{OUT} = 200mA$	—	220	—	
Line Regulation	$\frac{\Delta V_{OUT}}{\Delta V_{IN} \cdot V_{OUT}}$	$I_{OUT} = 40mA$ $(V_{set} + 1.0V) \leq V_{IN} \leq 8.0V$	—	0.05	—	%/V
Load Regulation	ΔV_{OUT}	$V_{IN} = V_{set} + 1.0V$ $1mA \leq I_{OUT} \leq 100mA$	—	50	—	mV
Current Limit	I_{LIMIT}		—	600	—	mA
Power Supply Rejection Rate	PSRR	$V_{IN} = V_{set} + 1.0V$ $f = 1KHz, I_{OUT} = 40mA$	—	75	—	dB
EN Threshold Voltage	V_{IL}	$V_{IN} = 3V \sim 5.5V$, Shutdown	—	—	0.4	V
	V_{IH}	$V_{IN} = 3V \sim 5.5V$, Start-Up	1.1	—	—	V
Output Noise Voltage	e_{NO}	$I_{OUT} = 40mA$ $BW = 300Hz \sim 50kHz$	—	50	—	μV_{RMS}
Output Voltage Temperature Coefficient	$\frac{\Delta V_{OUT}}{\Delta T \cdot V_{OUT}}$	$I_{OUT} = 10mA$	—	100	—	ppm/ $^\circ C$

Function Block Diagram



Application Guideline

Input Capacitor

A 1 μ F ceramic capacitor is recommended to connect between V_{DD} and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both VIN and GND.

Output Capacitor

An output capacitor is required for the stability of the LDO. The recommended output capacitance is 1 μ F, ceramic capacitor is recommended, and temperature characteristics are X7R or X5R. Higher capacitance values help to improve load/line transient response. The output capacitance may be increased to keep low undershoot/overshoot. Place output capacitor as close as possible to VOUT and GND pins.

Dropout Voltage

The dropout voltage refers to the voltage difference between the VIN and VOUT pins while operating at specific output current. The dropout voltage V_{DROP} also can be expressed as the voltage drop on

the pass-FET at specific output current (I_{RATED}) while the pass-FET is fully operating at ohmic region and the pass-FET can be characterized as a resistance $R_{DS(ON)}$. Thus the dropout voltage can be defined as ($V_{DROP} = V_{IN} - V_{OUT} = R_{DS(ON)} \times I_{RATED}$). For normal operation, the suggested LDO operating range is ($V_{IN} > V_{OUT} + V_{DROP}$) for good transient response and PSRR ability. Vice versa, while operating at the ohmic region will degrade the performance severely.

Thermal Application

For continuous operation, do not exceed the absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated as below: $T_A=25^{\circ}\text{C}$, PCB,

The max PD = $(125^{\circ}\text{C} - 25^{\circ}\text{C}) / (\text{Thermal Resistance } ^{\circ}\text{C/W})$

Power dissipation (PD) is equal to the product of the output current and the voltage drop across the output pass element, as shown in the equation below:

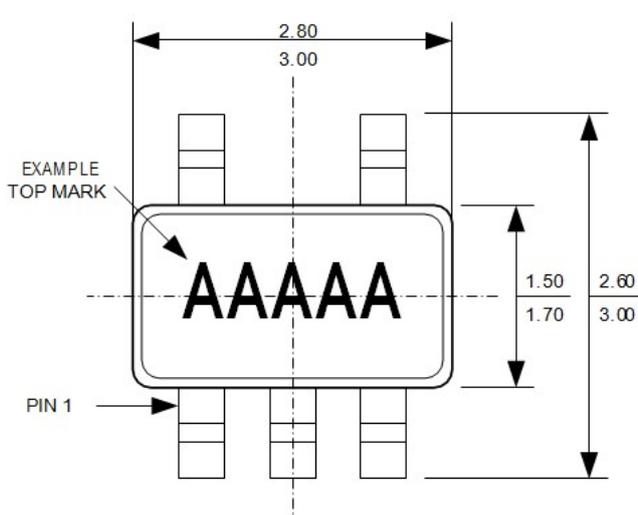
$$PD = (V_{IN} - V_{OUT}) \times I_{OUT}$$

Layout Consideration

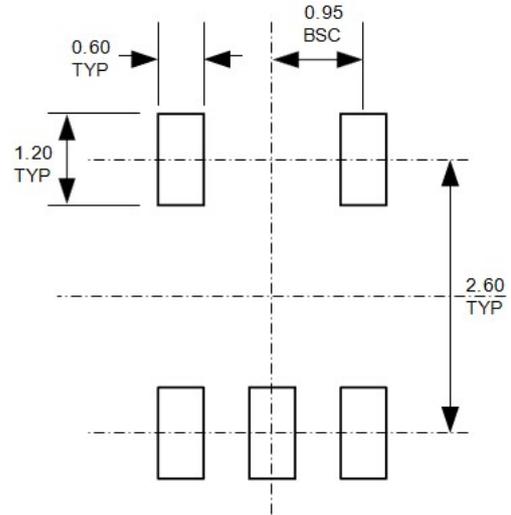
By placing input and output capacitors on the same side of the PCB as the LDO, and placing them as close as is practical to the package can achieve the best performance. The ground connections for input and output capacitors must be back to the HE2211 ground pin using as wide and as short of a copper trace as is practical. Connections using long trace lengths, narrow trace widths, and/or connections through via must be avoided. These add parasitic inductances and resistance that results in worse performance especially during transient conditions.

Packaging Information

SOT23-5



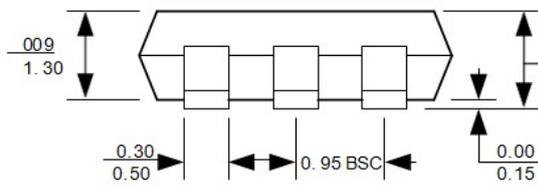
TOP VIEW



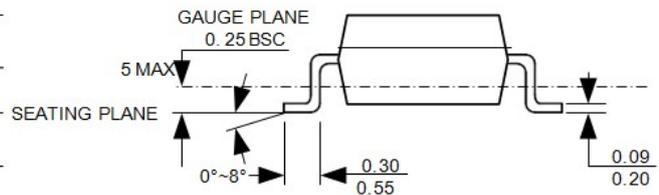
RECOMMENDED PAD LAYOUT

TOP VIEW

RECOMMENDED PAD LAYOUT



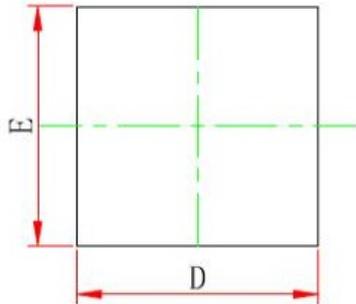
FRONT VIEW



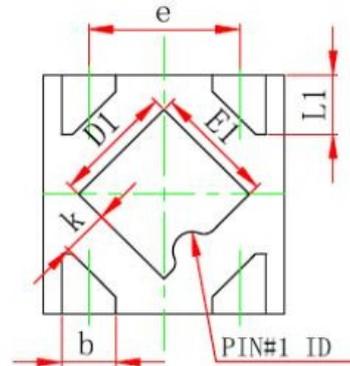
SIDE VIEW

Packaging Information

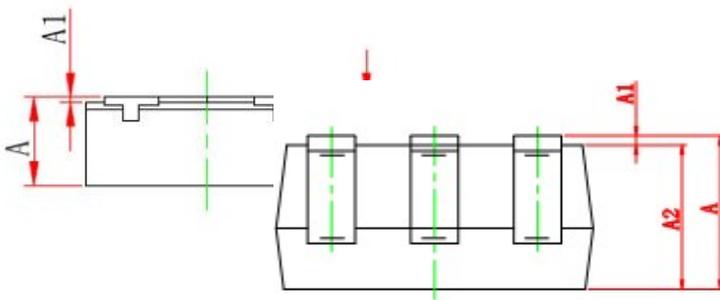
DFN1x1-4



TOP VIEW
[顶视图]



BOTTOM VIEW
[背视图]



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.335	0.405	0.013	0.016
A1	0.000	0.050	0.000	0.002
A2	0.100REF.		0.004REF.	
D	0.950	1.050	0.037	0.041
E	0.950	1.050	0.037	0.041
D1	0.450	0.550	0.018	0.022
E1	0.450	0.550	0.018	0.022
k	0.195REF.		0.0077REF.	
b	0.175	0.275	0.007	0.011
e	0.575	0.675	0.023	0.027
L1	0.200	0.300	0.008	0.012